Exhibit A

Netlist's P.R. 4-3 Statement[1]

A. 8,787,060 and 9,318,160

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
'160, all asserted claims	"the second driver size being different from the first driver size"	Plain and ordinary meaning, that is, the size of the second driver being different from the size of the first driver	**Exemplary Intrinsic Evidence** '060, 2:8-15 ("Generally, a load exists on each of the drivers 134, 140, 184, and 186 by virtue of the drivers being in electrical communication with the corresponding die interconnects and the corresponding circuitry of the array dies. Thus, to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver. However, generally a larger driver not only consumes more space on the control die, but also consumes more power."). '060, 4:22-29 ("In certain embodiments, reducing one or both of driver size and driver power consumption may be accomplished by increasing the number of die interconnects and reducing the number of array dies that are in electrical communication with each die interconnect. For example, instead of one die interconnect in electrical communication with four array dies, there may be two die interconnects, each in electrical communication with a different pair of the four array dies."). '060, 11:6-11 ("The size of the drivers 334 is generally related to the load on the driver 334. In certain embodiments, the load on

[1] Listed claims also include all claims dependent thereon, even if those claims are not separately listed. Netlist reserves the right to rely on intrinsic evidence cited by Micron.

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			each driver 334 corresponds to the load of the respective conduit 332. Although not limited as such, the load may be measured as a capacitive load, such as a parasitic capacitance."). '060, 17:37-49 ("The process 500 further comprises selecting a driver size for a first driver at block 508 and selecting a driver size for a second driver at block 510. Selecting the driver size can be based, at least in part, on the calculated load on the driver. Generally, the greater the load on the driver, the larger the driver is selected to drive a signal along, for example, a die interconnect. The size of the driver may be adjusted by the selection of the transistor size and/or number of transistors included in the driver. A larger driver often consumes more power than a smaller driver. Thus, in certain embodiments, balancing the loads on the drivers to reduce the load on each driver can reduce the power consumption of a memory package."). '060, 17:50-59 ("In some embodiments, the size of the first driver and the size of the second driver are both less than the size sufficient for a driver to drive a signal along a die interconnect to each of the array dies 310 (e.g., with less than a predetermined or threshold signal degradation). The threshold signal degradation can be based on any one or more characteristics of a signal. For example, the threshold signal degradation can be based on the amplitude of the signal, the frequency of the signal, the noise distortion included in or introduced into the signal, or the shape of the signal, to name a few.").

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			See also '060, 13:19-34, 13:34-47, 13:48-14:46. **Exemplary Extrinsic Evidence** Netlist may rely on expert testimony to explain the technology, the state of the art at the time the application leading to the '060/'160 patents was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. Netlist may also rely on the expert to respond to Micron's claim construction positions and any testimony of Micron's expert(s) and witnesses.

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
'060, claim 7	"The memory package of claim 1, wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect and a load of the second die interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit, the first load including a load of the first die interconnect, and a load of the first group of array dies, and the second load	Not indefinite	**Exemplary Intrinsic Evidence** '060, 2:8-15 ("Generally, a load exists on each of the drivers 134, 140, 184, and 186 by virtue of the drivers being in electrical communication with the corresponding die interconnects and the corresponding circuitry of the array dies. Thus, to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver. However, generally a larger driver not only consumes more space on the control die, but also consumes more power."). '060, 2:61-3:15 ("In certain embodiments, a method is provided for optimizing load in a memory package. The memory package comprises a plurality of array dies, at least a first die interconnect and a second die interconnect, and a control die. The control die comprises at least a first driver and a second driver, the first driver configured to drive a signal along the first die interconnect, and the second driver configured to drive the signal along the second die interconnect. The method comprises selecting a first subset of array dies of the plurality of array dies and a second subset of array dies of the plurality of array dies. The first subset of array dies and the second subset of array dies are exclusive of one another and are selected to balance a load on the first driver and on the second driver based at least in part on array die loads of array dies of the plurality of array dies and at least in part on die interconnect segment loads of segments of at least the first die interconnect and the second die interconnect. The method further comprises forming electrical connections between the first die interconnect and the first subset of array dies. In addition, the method comprises forming electrical connections between the second die interconnect and the second

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
	including a load of the second die interconnect and a load of the second group of at least one array die."		subset of array dies."). ’060, 4:30-54 ("In certain embodiments, determining the number of die interconnects and the number of array dies in electrical communication with each die interconnect is based, at least in part, on a load of each array die and a load of the die interconnect that is in electrical communication with one or more of the array dies. [¶] In some embodiments, the load contribution from a die interconnect may be negligible compared to the load contribution from the array dies. In such embodiments, determining the number of die interconnects and the number of array dies in electrical communication with each die interconnect may be based, at least in part, on a load of each array die without considering the load of the die interconnect. However, as the physical size of a memory package shrinks, the load of a die interconnect becomes a non-negligible value relative to the load of the array dies. Thus, as memory packages become physically smaller, it becomes more important to consider the load of the die interconnect in determining the number of die interconnects and the number of array dies in electrical communication with each die interconnect. Advantageously, certain embodiments of the present disclosure account for both the loads of the array dies and the loads of the die interconnects on a conduit (e.g., driver) in determining the number of die interconnects to be used and the number of array dies in electrical communication with each die interconnect"). ’060, 7:30-62 ("In some implementations, the difference between the load of the data conduit 232a and the load of the data conduit 232b is less than the maximum load for a data conduit as described

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			above. Thus, in Some cases, there may exist a degree of balance or equalization between the loads of the data conduits 232a, 232b. In some implementations, the difference between the load of the data conduit 232a and the load of the data conduit 232b is zero or substantially zero. In some embodiments, the length of each die interconnect 220, and the number of array dies 210 in electrical communication with each die interconnect 220 may be selected to maintain the difference between the load of the data conduit 232a and the load of the data conduit 232b to be at or below a threshold load difference. For example, suppose that the load of each array die 210 is 1, the load of each segment of the die interconnects 220 is 0.25, and that the threshold load difference is 0.5. Using the configuration schematically illustrated in FIG. 2, the load on the data conduit 232a in this example is 2.5 and the load on the data conduit 232b in this example is 3. Thus, in this example, the difference between the load of the data conduit 232a and the load of the data conduit 232b is at the threshold load difference value of 0.5. However, an alternative configuration that places the die interconnect 220a in electrical communication with only the array die 210a, and the die interconnect 220b in electrical communication with the array dies 210b-210d would not satisfy the threshold load difference value of 0.5 of the above example. In the alternative configuration, the load on the data conduit 232a would be 1.25 and the load on the data conduit 232b would be 4. Thus, in the alternative configuration, the difference between the load of the data conduit 232a and the load of the data conduit 232b is 2.75, which is above the threshold load difference value of 0.5.")

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			See also '060, 11:41-60, 14:4-21, 14:22-46, 16:42-55, 17:4-23, Fig. 5. **Exemplary Extrinsic Evidence** Netlist may rely on expert testimony to explain the technology, the state of the art at the time the application leading to the '060/'160 patents was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. The expert may also testify that in the context of the '060/'160 patents, a person of ordinary skill in the art would not view the claim as indefinite as Micron appears to contend. Netlist may also rely on the expert to respond to Micron's claim construction positions and any testimony of Micron's expert(s) and witnesses.

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
'060, all asserted claims; '160, all asserted claims	"die interconnect[s] in electrical communication with the . . . group of array dies and not in electrical communication with the . . . group"	Plain and ordinary meaning, that is, "electrical communication" that is different from "electrical connection"	**Exemplary Intrinsic Evidence** '060, 5:41-45 ("Each of the array dies 210 may include one or more data ports (not shown). The data ports enable electrical communication and data transfer between the corresponding memory circuitry of the array dies 210 and a communication pathway (e.g., a die interconnect)."); *see also* 5:54-6:35 ("Each of these die interconnects 220 may be coupled to, or in electrical communication with at least one data port of at least one of the array dies 210. In certain embodiments, at least one of the die interconnects 220 is in electrical communication with at least one data port from each of at least two array dies 210 without being in electrical communication with a data port from at least one array die 210, which may be in electrical communication with a different die interconnect 220.[¶] For example, die interconnect 220 a may be in electrical communication with a data port from array die 210a and a data port from array die 210b (as illustrated by the darkened circles in FIG. 2) and not in electrical communication with any data ports from array die 210c or any data ports from array die 210d. The data ports of array dies 210a and 210b in electrical communication with the die interconnect 220 a can be corresponding to the same data bit (e.g., D0). Other die interconnects (not shown) can be in electrical communication with other data ports corresponding to other data bits (e.g., D1, D2, . . .) of array dies 210a and 210b. These other die interconnects can be electrically isolated from the corresponding data ports of array dies 210c and 210d. [¶] However, continuing this example, the die interconnect 220 b may be in electrical communication with a data port from array die 210c and a data port from array die 210d (as

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			illustrated by the darkened circles in FIG. 2) (e.g., corresponding to the same data bit, e.g., D0) without being in electrical communication with any data ports from array die 210a and array die 210b. Other die interconnects (not shown) can be in electrical communication with other data ports corresponding to other data bits (e.g., D1, D2, . . .) of array dies 210c and 210d. Despite not being in electrical communication with any data ports from array die 210a and 210b, in some implementations, the die interconnect 220 b may pass through the array dies 210a and 210b (as illustrated by the unfilled circles) e.g., through through-holes or vias of array dies 210a and 210b. For some implementations, each of the array dies 210 may be in electrical communication with corresponding die interconnects 220, without any of the die interconnects 220 being in electrical communication with all of the array dies 210. Where existing systems may utilize a single die interconnect to be in electrical communication with the corresponding data ports of each array die (e.g., the data ports corresponding to the same bit), certain embodiments described herein utilize multiple die interconnects to provide electrical communication to the corresponding data ports of the array dies (e.g., the data ports corresponding to the same data bit) with none of the multiple die interconnects in electrical communication with data ports of all the array dies.). '060, 8:53-62 ("In certain embodiments, the TSV for array dies that are configured to be in electrical communication with the die interconnect and for array dies that are not configured to be in electrical communication with the die interconnect may be configured the same. However, in such cases, electrical

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			connections leading from the TSV of the array dies that are not configured to be in electrical communication with the die interconnect may not exist or may be stubs. These stubs are not configured to provide electrical communication with the memory cells of the array die."); *see also* 8:35-53. *See also* '060, Figs. 2-3, 6:36-67, 10:35-67, 11:12-31. **Exemplary Extrinsic Evidence** Netlist may rely on expert testimony to explain the technology, the state of the art at the time the application leading to the '060/'160 patents was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. Netlist may also rely on the expert to respond to Micron's claim construction positions and any testimony of Micron's expert(s) and witnesses.

B. 10,860,506

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
'506, claims 1-3, 11, 15, 16	"one or more previous operations"	one or more previous memory operations	**Exemplary Intrinsic Evidence** '506, 3:29-38 ("The memory module is operable to perform memory operations in response to memory commands (e.g., read, write, refresh, precharge, etc.), each of which is represented by a set of control/address (C/A) signals transmitted by the memory controller to the memory module. The C/A signals may include, for example, a row address strobe signal (/RAS), a column address strobe signal (/CAS), a write enable signal (/WE), an output enable signal (/OE), one or more chip select signals, row/column address signals, and bank address signals."); *see also* 5:11-26. '506, 3:40-44 ("In one embodiment, the C/A signals and the system clock signal are received by the module control device, which generates a set of module command signals and a set of module control signals in response to each memory command from the memory controller. The module command signals are transmitted by the module control device to the memory devices via module C/A signal lines, and the module control signals (referred sometimes herein as module control signals) are transmitted by the module control device to the buffer circuits via module control signal lines."). *See also* '506, 2:17-27, 2:28-31, 2:31-36, 4:9-19; 10:11-21, 8:21-34, 8:47-55, 9:51-62, 15:17-26, 15:27-50, 15:66-16:9, Figs. 12A and 12B.

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			Exemplary Extrinsic Evidence Netlist may rely on expert testimony to explain the technology, the state of the art at the time the application leading to the '506 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. The expert may testify that in the context of the '506 patent, a person of ordinary skill in the art would understand the term "one or previous operations" to mean "one or previous memory operations." Netlist may also rely on the expert to respond to Micron's claim construction positions and any testimony of Micron's expert(s) and witnesses. JEDEC Standard, DDR3 SDRAM Specification, JESD79-3A, September 2007. JEDEC Standard, DDR4 SDRAM Specification, JESD79-4, September 2012.
'506, claim 14	"before receiving the input C/A signals corresponding to the memory read operation, determining the first predetermined amount based at	The step of "determining the first predetermined amount based as least on signals received by the first data buffer" occurs before the earlier re-cited step of	**Exemplary Intrinsic Evidence** *See supra* evidence cited for "one or more previous operations." *See also* Fig. 18 and accompanying description at 18:6-64 ("Thus, as shown in FIG. 18, in one embodiment, a memory module 110 operates in the memory system 100 according to a method 1800. In the method, during a write operation, one or more module control signals are received by an isolation device 118 from a

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
	least on signals received by the first data buffer"	"receiving . . . input C/A signals"	module control circuit or module controller 116 (1810). The module controller 116 generates the one or more module control signals in response to C/A signals representing a write command from the MCH 101. The one or more module control signals are used to control the isolation device 118. For example, the one or more module control signals may include one or more first enable signals to enable a write path to allow write data be communicated to a selected subgroup of memory devices among the group of memory devices coupled to the isolation device 118. After a time interval from receiving the one or more first enable signals, write data DQ and write strobe DQS are received by the isolation device 118 from the MCH 101 (1820). In one embodiment, upon receiving the one or more first enable signal, a counter is started, which is stopped when the write data DQ or write strobe DQS is received. Thus, a time interval EWD between receiving the one or more first enable signals and receiving the write strobe signal DQS is recorded.[¶] Since the time interval between the arrival of the command signals from the MCH 101 and the arrival of the write data/strobe signal DQ/DQS from the MCH 101 is a set according to a write latency parameter associated with the system 100, the time interval EWD can be used to ascertain a time interval CED between the time when a command signal is received by the memory module 110 and the time when the one or more enable signals are received by the isolation device 118. The time interval CED can be used by the isolation device 118 to properly time the transmission of read data to the MCH 101, as described above and explained further below.[¶] As shown in FIG. 18, a delay signal DS is generated according to the time interval EWD (1830). Concurrent to receiving the write strobe signal DQS, the isolation

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			device 118 also receives a set of write data signals DQ (1840). The received write data signals are transmitted to the subgroup of memory devices (1850), which are selected from the group of memory devices coupled to the isolation device 118 by the one or more first enable signals.[¶] During a read operation, another set of module control signals including, for example, one or more second enable signals, are received by the isolation device 118 from the module controller 116 (1860). The one or more second enable signals are generated by the module controller 116 in response to read command signals received from the MCH 101, and are used by the isolation device 118 to select a subgroup of memory devices from which to receive read data. Afterwards, a read strobe signal DQS and a set of read data signal DQ are received from the selected subgroup of memory devices (1870). To properly time the transmission of the DQS and DQ signals to the MCH 101, the DQS and DQ signals are adjusted (e.g., delayed) according to the delay signal DS, such that the DQS and DQ signals follow a read command by a time interval consistent with a read latency parameter associated with the system 100."). *See also, id.*, 3:29-34, 4:9-19, 10:11-21, 15:27-16:24, FIGs. 12A-12B; 2020-10-16 Amendment after Notice of Allowance, at 2-10. **Exemplary Extrinsic Evidence** Netlist, Inc. v. Samsung Electronics Co., Ltd. et al., No. 2:21-cv-463-JRG (E.D. Tex.), Dkt. 114 ("Samsung I Markman Order"), at 14-16, 34.

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			Netlist may rely on expert testimony to explain the technology, the state of the art at the time the application leading to the '506 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. Netlist may also rely on the expert to respond to Micron's claim construction positions and any testimony of Micron's expert(s) and witnesses.

C. 10,949,339

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
'339, claim 1	"to actively drive a respective byte-wise section of the N-bit wide write data"	to "drive" means "enabling only one of the data paths while the other possible paths are disabled" (i.e., no further construction necessary)	**Exemplary Intrinsic Evidence** '339, Fig. 1A, 4:49-5:3, 5:23-28 (single-line two-rank prior art RDIMMs suffered from the excess load problem). '339, Fig. 2A and 5:45-64 ("Specifically, FIG. 2A shows a conventional memory subsystem 200 with at least one two-rank memory module 210, only one of which is shown for clarity. Each rank of the memory module 210 comprises a plurality of memory devices 212, such as dynamic random access memory (DRAM) devices or synchronous DRAM (SDRAM) devices. A register 230 receives a plurality of control lines 240 (shown as a single solid line) from the system memory controller 220 and is connected via control lines 242 to the memory devices 212 of each rank of the memory module 210. This memory subsystem 200 connects each data line of an array of data lines 250 (shown as dashed lines) from a system memory controller 220 to corresponding memory devices 212 in the two ranks in each memory module 210. Therefore, during a write operation, the system memory controller 220 sees all the memory devices 212 as its load via the data lines 250, and during a read operation, each memory device 212 sees multiple other memory devices 212, as well as the system memory controller 220, as its load via the data lines 250."). '339, 9:44-52 ("In certain embodiments, the memory devices 412, 412′ of the memory module 402, 402′ are arranged in four ranks, although embodiments with less than four ranks (e.g., one rank,

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			two ranks, three ranks) or more than four ranks (e.g., 6 ranks, 8 ranks) per memory module 402, 402′ may be employed. In certain embodiments, each rank comprises eight or nine memory modules, while in certain other embodiments, other numbers of memory modules per rank may also be used."). '339, 14:59-15:21 ("To reduce the memory device loads seen by the system memory controller 420 (e.g., during a write operation), the data transmission circuit 416 of certain embodiments is advantageously configured to be recognized by the system memory controller 420 as a single memory load. This advantageous result is desirably achieved in certain embodiments by using the data transmission circuits 416 to electrically couple only the enabled memory devices 412 to the memory controller 420 (e.g., the one, two, or more memory devices 412 to which data is to be written) and to electrically isolate the other memory devices 412 from the memory controller 420 (e.g., the one, two, or more memory devices 412 to which data is not to be written). …. In the example of FIG. 3A, during a write operation in which data is to be written to two memory device 412 in two ranks (e.g., memory devices 412A and 412C or memory devices 412B and 412D), each 15 data bit from the system memory controller 420 sees a single load from the memory module 402, which is presented by one of the data transmission circuits 416, instead of concurrently seeing the loads of all of the four memory devices 412A, 412B, 412C, 412D to which the data transmission 20 circuits 416 is operatively coupled.").

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			'339, 17:14-44 ("Referring again to FIG. 3A, when the memory controller 420 executes read or write operations, each specific operation is targeted to a specific one of the ranks A, B, C, and D of a specific memory module 402. The data transmission circuit 416 on the specifically targeted one of the memory modules 402 functions as a bidirectional repeater/multiplexor, such that it drives the data signal when connecting from the system memory controller 420 to the memory devices 412. The other data transmission circuits 416 on the remaining memory modules 402 are disabled for the specific operation. For example, the data signal entering on data line 518 entering into data transmission circuit 416 is driven to memory devices 412A and 412C or 412B and 412C depending on which memory devices are active and enabled. The data transmission circuit 416 then multiplexes the signal from the memory devices 412A, 412B, 412C, 412D to the system memory controller 420. The data transmission circuits 416 may each control, for example, a nibble-wide data path or a bytewide-data path. As discussed above, the data transmission circuits 416 associated with each module 402 are operable to merge data read signals and to drive data write signals, enabling the proper data paths between the system memory controller 420 and the targeted or selected memory devices 412. Thus, the memory controller 420, when there are four four-rank memory modules, sees four load-reducing switching circuit loads, instead of sixteen memory device loads. The reduced load on the memory controller 420 enhances the performance and reduces the power requirements of the memory system, as compared with, for example, the conventional systems described

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			above with reference to FIGS. 1A, 1B and 2A-2D."). *See also* '339, 8:31-53, 14:15-18 10:54-13:30, 13:31-53, 14:18-33, 14:34-55, 15:26-33, 10:43-46, 13:54-14:25, 15:26-40, 15:61-16:6, 15:13-18, 16:7-18:65; 10:54-11:4, Figs. 1A, 2A, 3A-3B, 4A-4B & associated text, Figs. 5-6. **Exemplary Extrinsic Evidence** Samsung I Markman Order, at 7-10, 34. To the extent Micron believes additional construction of the "drive" terms is necessary, Netlist reserves the right to rely on expert testimony in support of its constructions. Netlist may rely on expert testimony to explain the technology, the state of the art at the time the application leading to the '339 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. The expert may testify how a person of ordinary skill in the art would understand the term in the context of the '339 patent, and that the '339 patent provides detailed description on the structure and function of a byte-wise buffer as well the logic within the buffer. Netlist may also rely on the expert to respond to Micron's claim construction positions and any testimony of Micron's expert(s) and witnesses.

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
'339, claim 11	"to actively drive a respective section of the N-bit wide write data"	*See supra* '339 claim 1.	*See supra* evidence cited for '339 claim 1.
'339, claim 19	"actively drive a respective section of the [first/second] N-bit wide data"	*See supra* '339 claim 1.	*See supra* evidence cited for '339 claim 1.
'339, claim 27	"to drive the respective n-bit section of the [write/read] data"	*See supra* '339 claim 1.	*See supra* evidence cited for '339 claim 1.

D. 11,016,918 and 11,232,054[2]

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
'918, claims 1-3, 4-7, 913, 15, 21	"a second plurality of address and control signals"	plain and ordinary meaning (i.e., no further construction necessary)	**Exemplary Intrinsic Evidence** '918, 5:33-36, 21:65-22:34, 23:28-40, 23:41-24:8, 13:29-43, 16:56-17:13; Figs. 12-14, 15A-15C and accompanying description. **Exemplary Extrinsic Evidence** Samsung I Markman Order at 25-26, 35.
'918, claims 2, 17, 28; '054, claim 15	"dual buck converter" / "dual-buck converter"	"a buck converter with two regulated voltage outputs" (i.e., no further construction necessary)	**Exemplary Intrinsic Evidence** '918, 29:18-64; Fig. 16 and accompanying description. **Exemplary Extrinsic Evidence** Samsung I Markman Order at 18-21, 34.
'918, claims 16-22, 30	"pre-regulated input voltage" / "input voltage"	plain and ordinary meaning (i.e., no further construction necessary)	**Exemplary Intrinsic Evidence** '918, 27:59-28:2, 25:54-62, 26:8-35, 28:2-67, 30:35-45; Figures 12-14, 15A-C and 16, Fig. 17 and accompanying description. **Exemplary Extrinsic Evidence**

[2] Netlist does not believe that the terms of the '918/'054 patents that were construed in Samsung I require further construction at this time.

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			Samsung I Markman Order at 21-22, 34.
'918, all asserted claims	"first" / "second" / "third" / "fourth" "regulated voltages"	plain and ordinary meaning (i.e., no further construction necessary)	**Exemplary Intrinsic Evidence** '918, 26:36-43, 29:18-64, Figs. 12-14, 16 and accompanying description. **Exemplary Extrinsic Evidence** Samsung I Markman Order at 23-24, 34.
'918, all asserted claims	"first" / "second" / "third" / "fourth" "regulated voltage amplitude"	plain and ordinary meaning (i.e., no further construction necessary)	**Exemplary Intrinsic Evidence** '918, 26:36-43, 29:18-64, Figs. 12-14, 16 and accompanying description. **Exemplary Extrinsic Evidence** Samsung I Markman Order at 23-24, 34.
'054, claims 1–15	"at least three regulated voltages"	plain and ordinary meaning (i.e., no further construction necessary)	**Exemplary Intrinsic Evidence** '918, 26:36-43, 29:18-64, Figs. 12-14, 16 and accompanying description. **Exemplary Extrinsic Evidence** Samsung I Markman Order at 25, 34.

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
'054, claims 16, 24	"plurality of regulated voltages"	plain and ordinary meaning (i.e., no further construction necessary)	**Exemplary Intrinsic Evidence** '918, 26:36-43, 29:18-64, Figs. 12-14, 16 and accompanying description. **Exemplary Extrinsic Evidence** Samsung I Markman Order at 25, 35.
'918, all asserted claims '054, all asserted claims	"A memory module"	the preamble is limiting	**Exemplary Intrinsic Evidence** *See* '918, 3:66-7:67 ("Overview"), 9:66-10:1 ("Example embodiments are described herein in the context of a system of computers, servers, controllers, memory modules, hard disk drives and software."); *see also* 1:66-67. *See also*, '918, FIGs. 3A-B, 4A-B, 5A-B, 7, 8A-B, 9, 13, 14, 15A-C, and accompanying description at 11:11-21, 11:41-12:2, 12:26-29, 12:52-13:25, 22:52-23:27, 23:41-44. *See also, e.g.*, 21:24-55 ("In certain embodiments, the memory system 1010 comprises a memory module. The memory system 1010 may comprise a printed-circuit board (PCB) 1020. In certain embodiments, the memory system 1010 has a memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, or 8-GB. Other volatile memory capacities are also compatible with certain embodiments described herein. In certain embodiments, the memory system 10 has a non-volatile memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, 16-GB, or 32-GB. Other non-volatile memory capacities are also compatible with certain embodiments described herein. In

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			addition, memory systems 1010 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the PCB 1020 has an industry-standard form factor. For example, the PCB 1020 can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB 1020 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB 1020 has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FBDIMM), miniDIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein. For example, in other embodiments, certain non-DIMM form factors are possible such as, for example, single in-line memory module (SIMM), multi-media card (MMC), and small computer system interface (SCSI)."). *See also, e.g.*, '918 12:64-13:25 ("In certain embodiments, memory module 500 is a Flash-DRAM hybrid memory subsystem which may be integrated with other components of a host system. In certain embodiments, memory module 500 is a Flash-DRAM hybrid memory module that has the DIMM (dual-inline memory module) form factor, and may be referred to as a FDHDIMM, although it is to be understood that in both structure and operation it may be different from the FDHDIMM discussed above and described with reference to FIGS. 4A and 4B. Memory module

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			500 includes two on-module intermediary components: a controller and a data manager. These on-module intermediary components may be physically separate components, circuits, or modules, or they may be integrated onto a single integrated circuit or device, or integrated with other memory devices, for example in a three dimensional stack, or in any one of several other possible expedients for integration known to those skilled in the art to achieve a specific design, application, or economic goal. In the case of a DIMM, these on-module intermediary components are an on-DIMM Controller (CDC) 502 and an on-DIMM data manager (DMgr) 504**. While the DIMM form factor will predominate the discussion herein, it should be understood that this is for illustrative purposes only and memory systems using other form factors are contemplated as well**. CDC 502 and data manager DMgr 504 are operative to manage the interface between a non-volatile memory subsystem such as a Flash 506, a volatile memory subsystem such as a DRAM 508, and a host system represented by MCH 510."). **Exemplary Extrinsic Evidence** Samsung I Markman Order at 26-28, 35.

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
'918, all claims	"converter circuit"	Not subject to § 112(6); plain and ordinary meaning, i.e., a circuit for voltage conversion	**Exemplary Intrinsic Evidence** '918, 29:18-54 ("The conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters. The conversion element 1120 may comprise a plurality of sub-blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010. For example, in one embodiment, sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16. Various other components for the sub-blocks 1122, 1124, 1126 of the conversion element 1120 are also compatible with certain embodiments described herein. In certain embodiments, the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and reduces the input to an appropriate amount for powering various components of the memory system. For example, the buck-converter of sub-block 1122 can provide 1.8V at 2A for about 60 seconds to the volatile memory elements 1032 (e.g., DRAM), the non-volatile memory elements 1042 (e.g., flash), and the controller 1062 (e.g., an FPGA) in one embodiment. The sub-block 1124 can provide the second voltage 1104 as well as another reduced voltage 1105 to the memory system 1010. In one example embodiment, the second

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			voltage 1104 is 2.5V and is used to power the at least one circuit 1052 (e.g., isolation device) and the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052."); *see also* Fig. 16, 27:59-28:2. 29:55-64 ("Although described with respect to certain example embodiments, one of ordinary skill will recognize from the disclosure herein that the conversion element 1120 may include alternative embodiments. For example, there may be more or less sub-blocks which may comprise other types of converters (e.g., pure boost converters) or which may produce different voltage values. In one embodiment, the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are not both powered using the first voltage 1102."). 28:59-29:17 ("In certain embodiments, the second power element 1140 does not comprise a battery and may comprise one or more capacitors. For example, as schematically illustrated in FIG. 16, the second power element 1140 comprises a capacitor array 1142, a buck-boost converter 1144 which adjusts the voltage for charging the capacitor array and a voltage/current limiter 1146 which limits the charge current to the capacitor array 1142 and stops charging the capacitor array 1142 when it has reached a certain charge voltage. In one example embodiment, the capacitor array 1142 comprises two 50 farad capacitors capable of holding a

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			total charge of 4.6V. For example, in one example embodiment, the buck-boost converter 1144 receives a 1.8V system voltage (first voltage 1108) and boosts the voltage to 4.3V which is outputted to the voltage current limiter 1146. The voltage/current limiter 1146 limits the current going to the capacitor array 1142 to 1A and stops charging the array 1142 when it is charged to 4.3V. Although described with respect to certain example embodiments, one of ordinary skill will recognize from the disclosure herein that the second power element 1140 may include alternative embodiments. For example, different components and/or different value components may be used. For example, in other embodiments, a pure boost converter may be used instead of a buck-boost converter. In another embodiment, only one capacitor may be used instead of a capacitor array 1142."); *see also* 28:3-58. **Exemplary Extrinsic Evidence** Netlist may rely on expert testimony to explain the technology, the state of the art at the time the application leading to the '918/'054 patents was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. The expert may testify that in the context of the '918 patent, a person of ordinary skill in the art would understand the term "converter circuit" to mean "a circuit for voltage conversion."

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			Netlist may also rely on the expert to respond to Micron's claim construction positions and any testimony of Micron's expert(s) and witnesses. U.S. Patent Publication No. 2006/0174140 (Harris) The Penguin Dictionary of Electronics (4th ed. 2005) Dictionary of Science and Technology (2nd Ed. 2003) Wiley Electrical and Electronics Engineering Dictionary (2004) Chambers Dictionary of Science and Technology (2007) A Dictionary of Computing (6th ed., 2008) Second Edition Comprehensive Dictionary of Electrical Engineering (2005)

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
'918, claims 1-3, 5-7, 9-13, 15, 21	"at least one circuit"	Not subject to § 112(6); plain and ordinary meaning If subject to §112(6), then: Function: (i) receive a first plurality of address and control signals via [the first/a second] portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices Structures: As described in 21:14-23, 23:27-31, 23:41-24:8 or equivalents thereof.	**Exemplary Intrinsic Evidence** Figs. 12-14, 15A-C and accompanying description. 21:14-23 ("FIG. 12 is a block diagram of an example memory system 1010 compatible with certain embodiments described herein. The memory system 1010 can be coupled to a host computer system and can include a volatile memory subsystem 1030, a non-volatile memory subsystem 1040, and a controller 1062 operatively coupled to the non-volatile memory subsystem 1040. In certain embodiments, the memory system 1010 includes at least one circuit 1052 configured to selectively operatively decouple the controller 1062 from the volatile memory subsystem 1030."). 23:41-24:8 ("In certain embodiments, the volatile memory subsystem 1030 can comprise a registered DIMM subsystem comprising one or more registers 1160 and a plurality of DRAM elements 1180, as schematically illustrated by FIG. 15A. In certain such embodiments, the at least one circuit 1052 can comprise one or more switches 1172 coupled to the controller 1062 (e.g., logic element 1070) and to the volatile memory subsystem 1030 which can be actuated to couple and decouple the controller 1062 to and from the volatile memory subsystem 1030, respectively. The memory system 1010 further comprises one or more switches 1170 coupled to the one or more registers 1160 and to the plurality of DRAM elements 1180 as schematically illustrated by FIG. 15A. The one or more switches 1170 can be selectively switched, thereby selectively operatively coupling the volatile

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			memory subsystem 1030 to the host system 1150. In certain other embodiments, as schematically illustrated by FIG. 15B, the one or more switches 1174 are also coupled to the one or more registers 1160 and to a power source 1162 for the one or more registers 1160. The one or more switches 1174 can be selectively switched to turn power on or off to the one or more registers 1160, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system 1150. As schematically illustrated by FIG. 15C, in certain embodiments the at least one circuit 1052 comprises a dynamic on-die termination (ODT) 1176 circuit of the logic element 1070. For example, the logic element 1070 can comprise a dynamic ODT circuit 1176 which selectively operatively couples and decouples the logic element 1070 to and from the volatile memory subsystem 1030, respectively. In addition, and similar to the example embodiment of FIG. 15A described above, the one or more switches 1170 can be selectively switched, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system 1150."). *See also* 21:24-51, 22:1-8, 23:28-40, 24:60-25:31, 25:32-53. **Exemplary Extrinsic Evidence** Netlist may rely on expert testimony to explain the technology, the state of the art at the time the application leading to the '918/'054 patents was filed, the level of ordinary skill in the relevant art, and

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. Netlist may also rely on the expert to respond to Micron's claim construction positions and any testimony of Micron's expert(s) and witnesses. *See also* definitions of "circuit" in contemporary dictionaries cited above.
'054, claims 1-13, 15	"first circuit"	plain and ordinary meaning	*See supra* evidence cited for "at least one circuit."

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
'918, claims 12, 18-19, 25-26; '054, claims 5, 7-13, 16-17, 23-25, 29-30	"controller"	Not subject to § 112(6) and not indefinite; plain and ordinary meaning. To the extent that "controller" is a § 112(6) term, the function and corresponding structure vary for each claim, contrary to Micron's attempt to aggregate all functions into the term. Structures: As described in 23:1-27, 24:35-37, 25:8-31, 29:33-54, 32:49-51 or equivalents thereof.	**Exemplary Intrinsic Evidence** 25:8-31 ("The memory system 1010 may further comprise a voltage monitor 1050. The voltage monitor circuit 1050 monitors the voltage supplied by the host system via the interface 1022. Upon detecting a low voltage condition (e.g., due to a power interruption to the host system), the voltage monitor circuit 1050 may transmit a signal to the controller 1062 indicative of the detected condition. The controller 1062 of certain embodiments responds to the signal from the voltage monitor circuit 1050 by transmitting a signal to the at least one circuit 1052 to operatively couple the controller to the volatile memory system 1030, such that the memory system 1010 enters the second state. For example, the voltage monitor 1050 may send a signal to the MCU 1060 which responds by accessing the data on the volatile memory system 1030 and by executing a write cycle on the nonvolatile memory subsystem 1040. During this write cycle, data is read from the volatile memory subsystem 1030 and is transferred to the non-volatile memory subsystem 1040 via the MCU 1060. In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition."). 20:17-28 ("Certain embodiments described herein include a memory system which can communicate with a host system such as a disk controller of a computer system. The memory system can include volatile and non-volatile memory, and a controller. The controller backs up the volatile memory using the non-volatile

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			memory in the event of a trigger condition. Trigger conditions can include, for example, a power failure, power reduction, request by the host system, etc. In order to power the system in the event of a power failure or reduction, the memory system can include a secondary power source which does not comprise a battery and may include, for example, a capacitor or capacitor array."); 20:29-42. 23:1-27 ("Referring to FIG. 12, in certain embodiments, the logic element 1070 comprises a field-programmable gate array (FPGA). In certain embodiments, the logic element 1070 comprises an FPGA available from Lattice Semiconductor Corporation which includes an internal flash. In certain other embodiments, the logic element 1070 comprises an FPOA available from another vendor. The internal flash can improve the speed of the memory system 1010 and save physical space. Other types of logic elements 1070 compatible with certain embodiments described herein include, but are not limited to, a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, a complex programmable logic device (CPLD). In certain embodiments, the logic element 1070 is a custom device. In certain embodiments, the logic element 1070 comprises various discrete electrical elements, while in certain other embodiments, the logic element 1070 comprises one or more integrated circuits. FIG. 14 is a block diagram of an example memory module 1010 having a microcontroller unit 1060 and logic element 1070 integrated into a single controller 1062 in accordance with certain embodiments described herein. In certain embodiments, the controller 1062 includes one or

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			more other components. For example, in one embodiment, an FPGA without an internal flash is used and the controller 1062 includes a separate flash memory component which stores configuration information to program the FPGA."). *See also* 21:14-26:65, 29:33-54, 32:49-51, Figs. 12-14, Fig. 15A-C, Fig. 16 and accompanying description. *See also* '918 patent, 13:6-18 ("Memory module 500 includes two on-module intermediary components: a controller and a data manager. These on-module intermediary components may be physically separate components, circuits, or modules, or they may be integrated onto a single integrated circuit or device, or integrated with other memory devices, for example in a three dimensional stack, or in any one of several other possible expedients for integration known to those skilled in the art to achieve a specific design, application, or economic goal. In the case of a DIMM, these on-module intermediary components are an on-DIMM Controller (CDC) 502 and an on-DIMM data manager (DMgr) 504."). 17:59-18:17 ("In certain embodiments, a memory controller can access the memory module using a standard access protocol, such as JEDEC's DDR DRAM, by sending a memory access command to the CDC 502 which in turn determines what type of a data transfer operation it is and the corresponding target address where the data information is stored, e.g. data information is stored in the DRAM 508 or Flash 506 memory subsystems. In response to a read operation, if the CDC 502 determines that data information,

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			e.g. a page (or block), does not reside in the DRAM 508 but resides in Flash 506, then the CDC 502 initiates and controls all necessary data transfer operations from Flash 506 to DRAM 508 and subsequently to the memory controller. In one embodiment, once the CDC 502 completes the data transfer operation of the requested data information from the Flash 506 to the DRAM 508, the CDC 502 alerts the memory controller to retrieve the data information from the DRAM 508. In on embodiment, the memory controller initiates the copying of data information from Flash 506 to DRAM 508 by writing, into a register in the CDC 502, the target Flash address along with a valid block size. The CDC 502 in turn, executes appropriate operations and generates control information to copy the data information to the DRAM 508. Consequently, the memory controller can access or retrieve the data information using standard memory access commands or protocol."). **Exemplary Extrinsic Evidence** Netlist may rely on expert testimony to explain the technology, the state of the art at the time the application leading to the '918/'054 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. Netlist may also rely on the expert to respond to Micron's claim construction positions and any testimony of Micron's expert(s) and witnesses.

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			Dictionary of Science and Technology (2nd Ed. 2003) Wiley Electrical and Electronics Engineering Dictionary (2004) Second Edition Comprehensive Dictionary of Electrical Engineering (2005)

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
'054, claims 4, 6, 11, 16, 18, 19, 21, 25, 26	"first operable state" / "second operable state"	"first operable state" is a "state in which the memory module is operated before transition"; not indefinite "second operable state" is a "state in which the memory module is operated after transition"; not indefinite	**Exemplary Intrinsic Evidence** '918, 20:43-57 ("In certain embodiments described herein, the memory system includes a power module which provides power to the various components of the memory system from different sources based on a state of the memory system in relation to a trigger condition (e.g., a power failure). The power module may switch the source of the power to the various components in order to efficiently provide power in the event of the power failure. For example, when no power failure is detected, the power module may provide power to certain components, such as the volatile memory, from system power while charging a secondary power source (e.g., a capacitor array). In the event of a power failure or other trigger condition, the power module may power the volatile memory elements using the previously charged secondary power source."). '918, 24:60-25:7 ("The memory system 1010 of certain embodiments is configured to be operated in at least two states. The at least two states can comprise a first state in which the controller 1062 and the non-volatile memory subsystem 1040 are operatively decoupled (e.g., isolated) from the volatile memory subsystem 1030 by the at least one circuit 1052 and a second state in which the volatile memory subsystem 1030 is operatively coupled to the controller 1062 to allow data to be communicated between the volatile memory subsystem 1030 and the nonvolatile memory subsystem 1040 via the controller 1062. The memory system 1010 may transition from the first state to the second state in response to a trigger condition, such as when the memory

Claims	Terms for Construction	Netlist's Proposed Constructions	Exemplary Evidence
			system 1010 detects that there is a power interruption (e.g., power failure or reduction) or a system hang-up."); *see also* 25:8-27:13. 28:39-58 ("In certain embodiments, the power module 1100 transitions from the first state to the second state upon detecting that a trigger condition is likely to occur and transitions from the second state to the third state upon detecting that the trigger condition has occurred. For example, the power module 1100 may transition to the second state when it detects that a power failure is about to occur and transitions to the third state when it detects that the power failure has occurred. …."); *see also* 28:26-38, 30:50-64. **Exemplary Extrinsic Evidence** Netlist may rely on expert testimony to explain the technology, the state of the art at the time the application leading to the '918/'054 patent was filed, the level of ordinary skill in the relevant art, and the meaning of this claim element to a person of ordinary skill in the art at the time of the invention. Netlist may also rely on the expert to respond to Micron's claim construction positions and any testimony of Micron's expert(s) and witnesses.